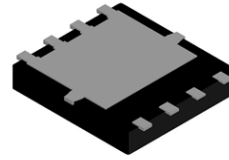


FEATURES

- Drain-Source Withstand Voltage: 40V
- Max. $R_{DS(on)}$: 2.7m Ω @ $V_{GS}=10V$
3.9m Ω @ $V_{GS}=4.5V$
- Trench Technology
- Supper high density cell design
- Low ON resistance
- Low Threshold Voltage
- Package PDFN3333-8L
- 100% UIS and Rg Tested

PRODUCT APPEARANCE

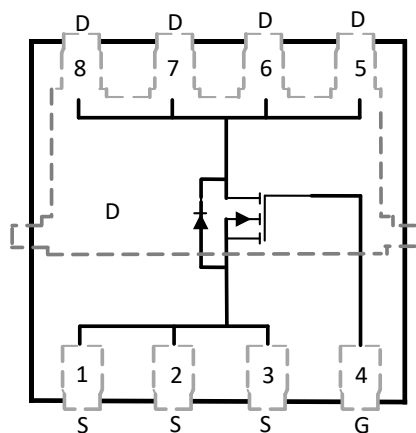
PDFN3333-8L

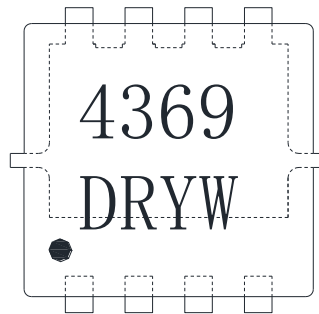
DESCRIPTION

The SNM042R7DRA is N-Channel enhancement MOS Field Effect Transistor. Uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in DC-DC conversion, power switch and charging circuit. Standard Product SNM042R7DRA is in compliance with RoHS.

Applications:

- DC/DC converters
- Power supply converters circuit
- Load/Power Switching for portable device

PIN CONFIGURATION

MARKING


4369 = Device Code
 DR = Special Code
 Y = Year
 M = Month (A~z)

LIMITING VALUES

Parameter	Symbol	Condition	Value	Unit
Drain-Source Voltage	V_{DS}		40	V
Gate-Source Voltage	V_{GS}		± 20	V
Continuous Drain Current ⁽⁴⁾	I_D	$T_C=25^\circ\text{C}$	137	A
		$T_C=100^\circ\text{C}$	86	A
Pulsed Drain Current ⁽³⁾	I_{DM}		359	A
Continuous Drain Current	I_D	$T_A=25^\circ\text{C}$	33	A
		$T_A=100^\circ\text{C}$	26	A
Avalanche Energy $L=0.3\text{mH}$	E_{AS}		256	mJ
Power Dissipation ⁽²⁾	P_D	$T_C=25^\circ\text{C}$	83	W
		$T_C=100^\circ\text{C}$	33	W
Power Dissipation ⁽¹⁾	P_D	$T_A=25^\circ\text{C}$	4.8	W
		$T_A=100^\circ\text{C}$	3.1	W
Operating Junction Temperature	T_J		-55 to 150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}		-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Single Operation					
Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient Thermal Resistance ⁽¹⁾	t ≤ 10s		20	26	°C/W
	Steady State	R _{θJA}	46	58	
Junction-to-Case Thermal Resistance	Steady State	R _{θJC}	1.2	1.5	

ELECTRONICS CHARACTERISTICS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0 V, I _D = 250μA	40			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 40V, V _{GS} = 0V			1	μA
Gate-to-source Leakage Current	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA	1.2	1.7	2.2	V
Drain-to-source On-resistance ⁽⁵⁾	R _{DS(on)}	V _{GS} = 10V, I _D = 20A		2.2	2.7	mΩ
		V _{GS} = 4.5V, I _D = 20A		3.0	3.9	
CHARGES, CAPACITANCES AND GATE RESISTANCE ⁽⁶⁾						
Input Capacitance	C _{ISS}	V _{GS} = 0V, f = 1.0MHz, V _{DS} = 25 V		2698		pF
Output Capacitance	C _{OSS}			582		
Reverse Transfer Capacitance	C _{RSS}			28		
Total Gate Charge	Q _{G(10V)}	V _{GS} = 10V, V _{DS} = 20V, I _D = 30A		37.4		nC
Total Gate Charge	Q _{G(4.5V)}			17.7		
Gate-to-Source Charge	Q _{GS}			7.2		
Gate-to-Drain Charge	Q _{GD}			4.1		
Gate Resistance	R _g	f = 1MHz		1.8		Ω
SWITCHING CHARACTERISTICS ⁽⁶⁾						

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Turn-On Delay Time	td(ON)	$V_{GS} = 20V,$ $V_{DS} = 10V,$ $I_D = 20A,$ $R_{GEN} = 1.6\Omega$		7.2		ns
Rise Time	tr			55.2		
Turn-Off Delay Time	td(OFF)			43.0		
Fall Time	tf			22.8		
BODY DIODE CHARACTERISTICS						
Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=20A$	0.5	0.8	1.2	V
Maximum Continuous Currents	I_S				64	A
Body Diode Reverse Recovery Time ⁽⁶⁾	trr	$I_F=20A,$ $di/dt= 100A/\mu s$		31.7		ns
Body Diode Reverse Recovery Charge ⁽⁶⁾	Qrr	$I_F=20A,$ $di/dt= 100A/\mu s$		22.5		nC

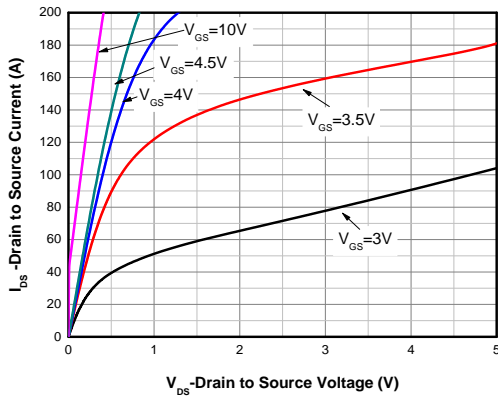
($T_J=25^\circ C$, unless otherwise noted.)

Note:

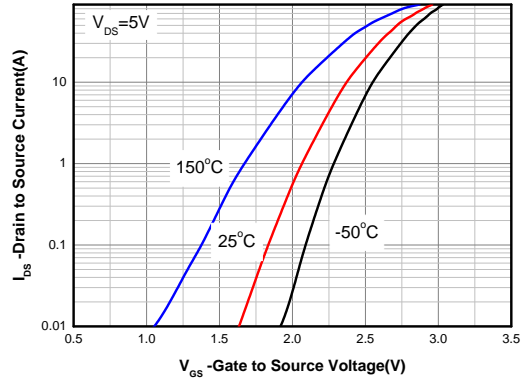
- (1) FR-4 board (38mm × 38mm × t1.6mm, 70μm Copper) partially covered with copper (645mm² area).
- (2) The power dissipation P_D is based on $T_{J(MAX)}=150^\circ C$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.
- (3) Repetitive rating, ~10us pulse width, duty cycle ~1%, keep initial $T_J=25^\circ C$, the maximum allowed junction temperature of 150°C.
- (4) The power dissipation P_{DSM} is based on Junction-to-Ambient thermal resistance $R_{\theta JA} t \leq 10s$ value and the $T_{J(MAX)}=150^\circ C$.
- (5) The static characteristics are obtained using ~380μs pulse, duty cycle ~1%.
- (6) The parameter is not subject to production test – verified by design / characterization.

TYPICAL CHARACTERISTICS

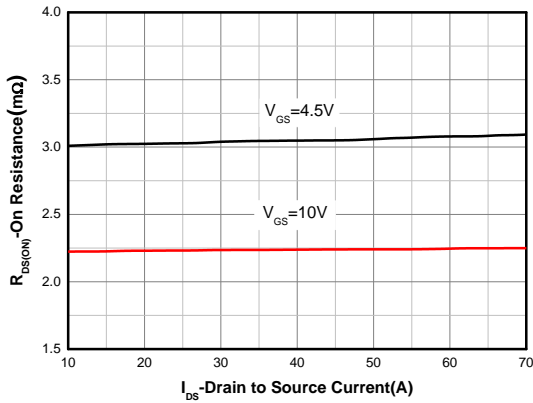
Ta=25°C, unless otherwise noted.



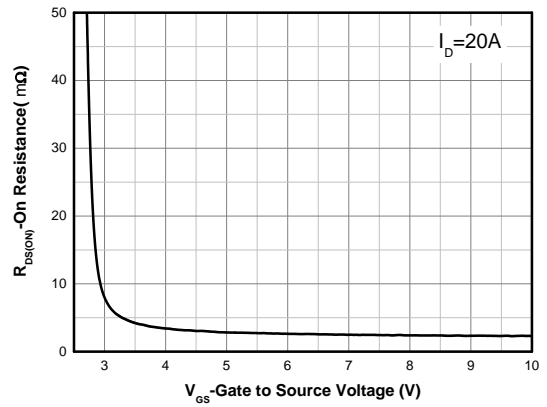
Output Characteristics ⁽⁵⁾



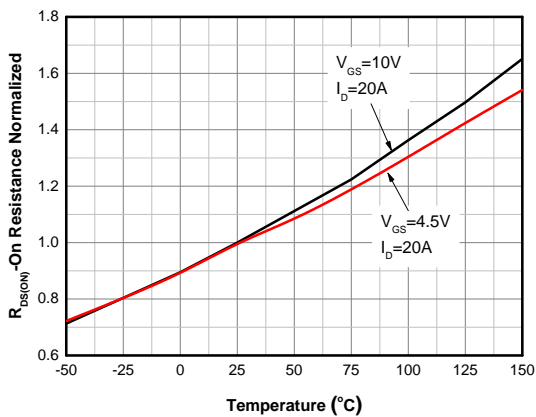
Transfer Characteristics ⁽⁵⁾



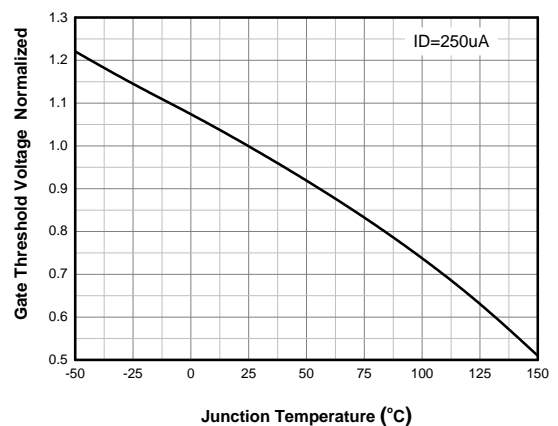
On-Resistance vs. Drain Current ⁽⁵⁾



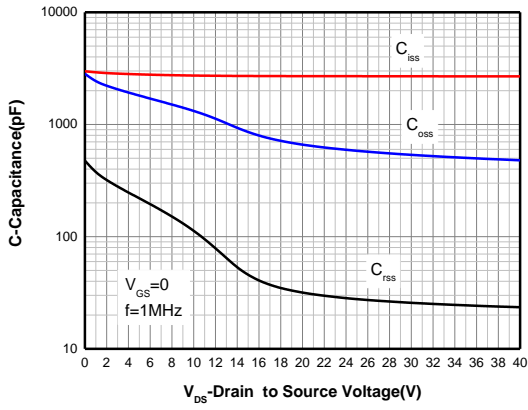
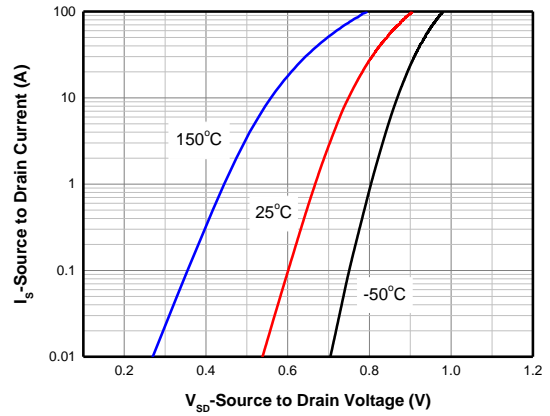
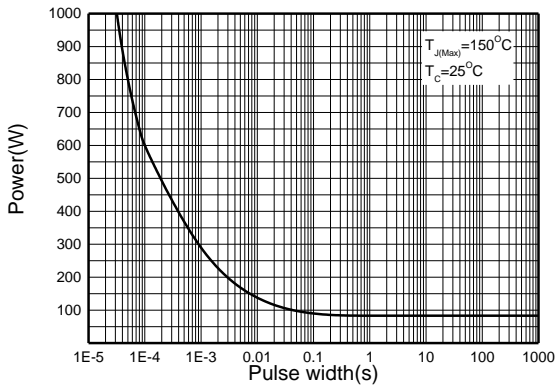
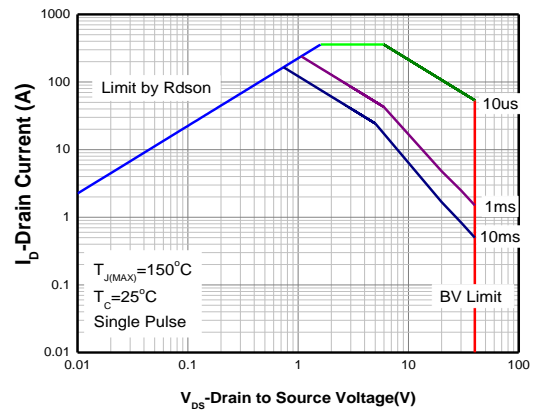
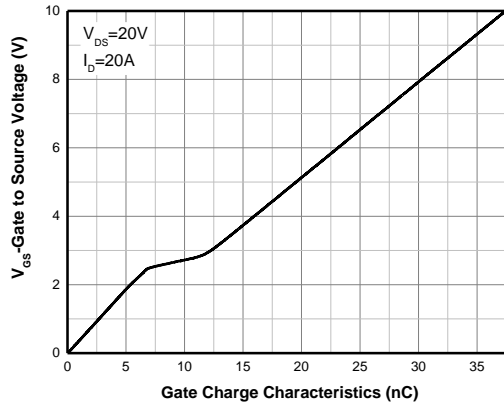
On-Resistance vs. Gate-to-Source Voltage ⁽⁵⁾

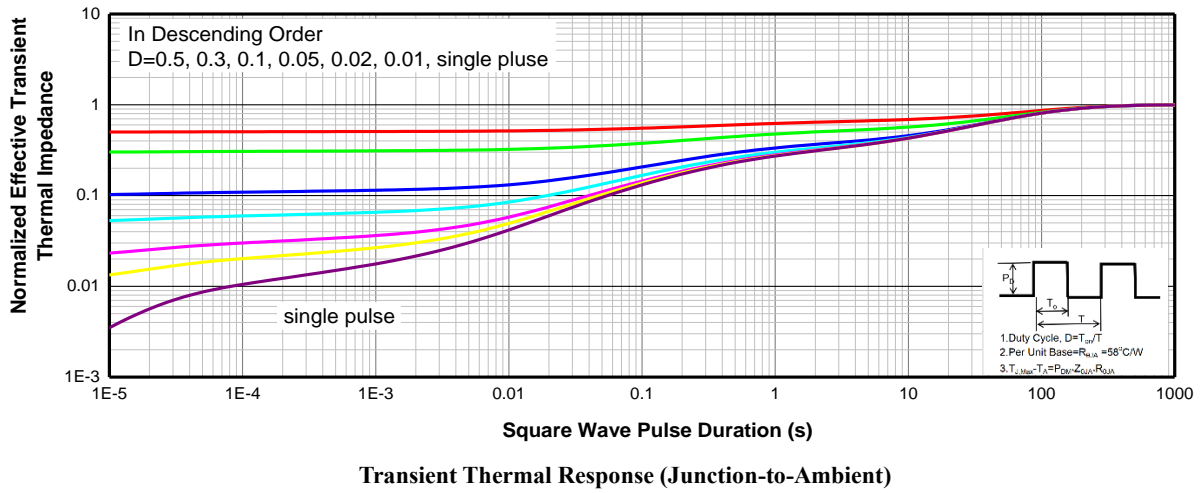
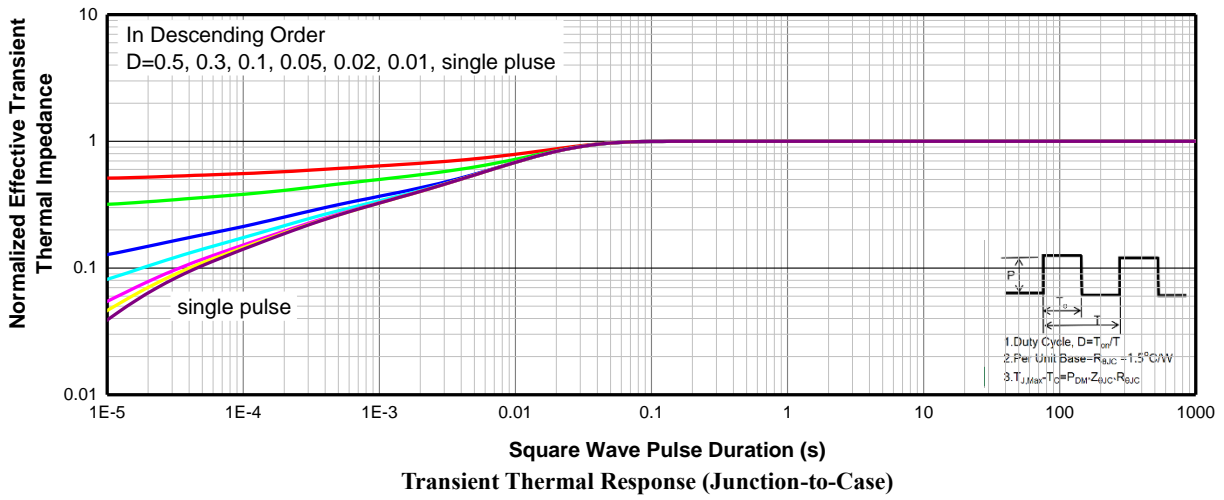


On-Resistance vs. Junction Temperature ⁽⁵⁾



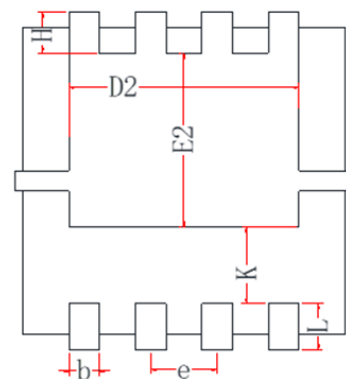
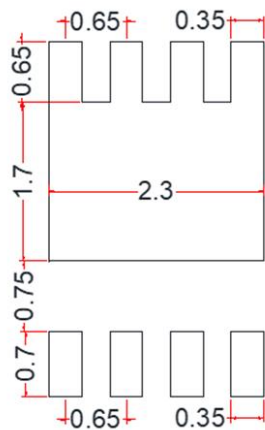
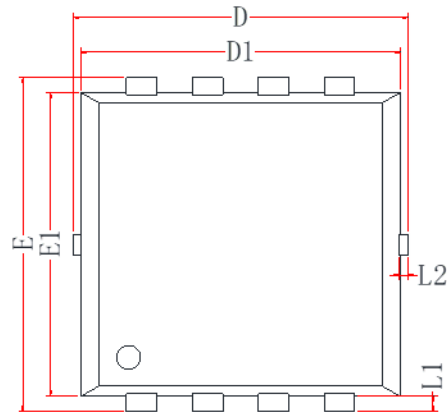
Threshold Voltage vs. Temperature

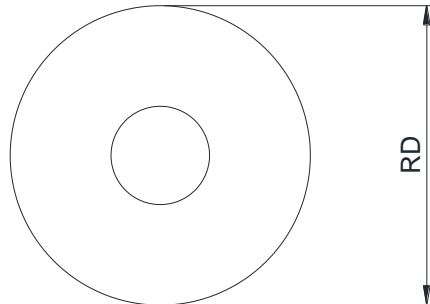
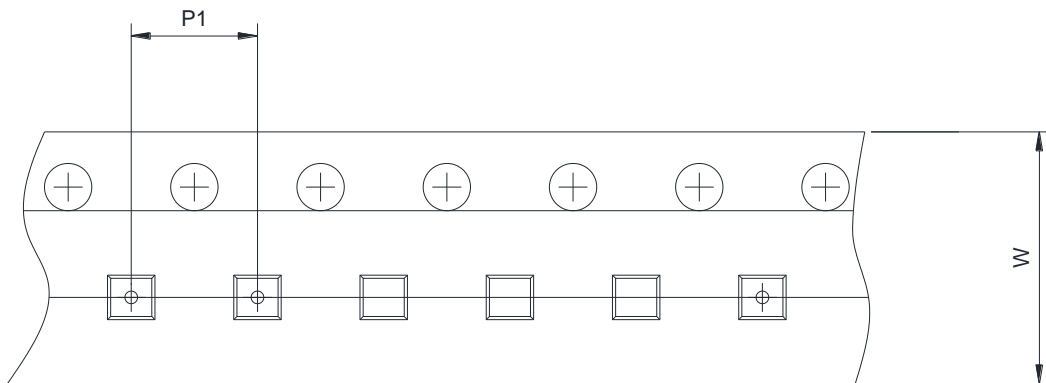
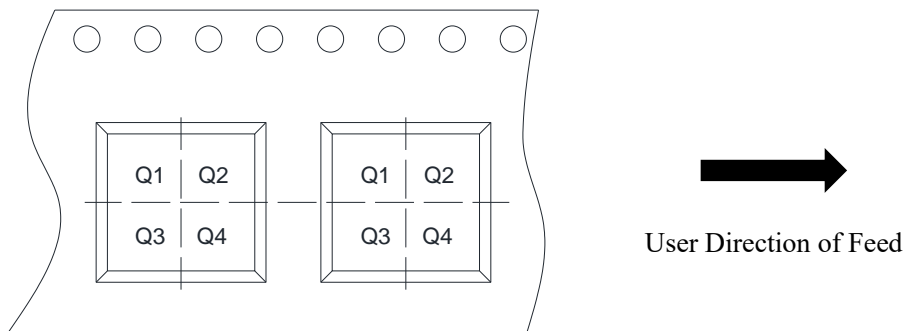

Capacitance

Body Diode Forward Voltage ⁽⁵⁾

Single Pulse power

Safe Operating Area

Gate Charge Characteristics



PDFN3333-8L DIMENSIONS
PACKAGE SIZE

Symbol	Min.	Typ.	Max.
A	0.70	0.80	0.90
b	0.25	0.30	0.39
c	0.14	0.15	0.20
D	3.10	3.30	3.50
D1	3.05	3.15	3.25
D2	2.15	2.25	2.35
e	0.55	0.65	0.75
E	3.10	3.30	3.50
E1	2.90	3.00	3.10
E2	1.60	1.70	1.80
H	0.25	0.40	0.55
K	0.65	0.75	0.85
L	0.30	0.45	0.60
L1	0.05	0.15	0.25
L2	-	-	0.15
θ	8°	10°	12°



TAPE AND REEL INFORMATION
Reel Dimensions

Tape Dimensions

Quadrant Assignments For PIN1 Orientation In Tape


RD	Reel Dimension	<input type="checkbox"/> 7inch	<input checked="" type="checkbox"/> 13inch
W	Overall width of the carrier tape	<input type="checkbox"/> 8mm	<input checked="" type="checkbox"/> 12mm <input type="checkbox"/> 16mm
P1	Pitch between successive cavity centers	<input type="checkbox"/> 2mm	<input type="checkbox"/> 4mm <input checked="" type="checkbox"/> 8mm
Pin1	Pin1 Quadrant	<input checked="" type="checkbox"/> Q1	<input type="checkbox"/> Q2 <input type="checkbox"/> Q3 <input type="checkbox"/> Q4

ORDERING INFORMATION

TYPE NUMBER	PACKAGE	PACKING
SNM042R7DRA-8/TR	PDFN3333-8L	Tape and reel

PDFN3333-8L is packed with 5000 pieces/disc in braided packaging.

Important statement

SIT reserves the right to change the above-mentioned information without prior notice.

REVISION HISTORY

Version number	Datasheet status	Revision date
V1.0	Initial version.	June 2024